## REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-16 and 19-24 are presently active in this case, Claims 1, 4, 8-10, and 15 having been amended, Claims 17 and 18 canceled, and Claims 20-24 added by the present amendment.

In the outstanding Official Action, Claims 16 and 18 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite; Claims 1-5, 7-10, 13, and 19 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 7,096,406 to Kanazawa et al. (hereinafter "Kanazawa"); Claims 6 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kanazawa in view of USP 6,339,546 to Katayama et al. (hereinafter "Kayatama"); and Claims 11, 14, 15, and 17 were objected to as being dependent upon a rejected base claim, but were otherwise indicated as including allowable subject matter if rewritten in independent form; and Claims 16 and 18 were also indicated as including allowable subject matter if rewritten in independent form and subject to overcoming the rejection under 35 U.S.C. §112, second paragraph.

Applicants acknowledge with appreciation the indication of allowable subject matter. However, since Applicants consider that the amended claims patentably define over the cited prior art, Claims 11 and 14-16 have been maintained in dependent form. Claims 17-18 have been canceled.

In response to the rejection under 35 U.S.C. §112, second paragraph, Claim 1 has been amended to include the "wherein" clause in the last paragraph of Claim 1. This "wherein" provides antecedent basis for "a write-enable signal which is input from the host," and accordingly the rejection of Claim 16 under 35 U.S.C. §112, second paragraph, has been

overcome. In view of the cancellation of Claim 18, the outstanding rejection of Claim 18 is moot.

In light of the outstanding rejection based on 35 U.S.C. §102, Claim 1 has been amended to clarify the claimed invention and thereby more clearly patentably define over the cited prior art. In amended claim 1, both "a first input/output circuit" and "a second input/output circuit" in original claim 1 are represented together as "a data-path circuit." The data-path circuit is limited to operate in synchronization with a first clock. The first clock corresponds to "WE_CLK" shown in FIG. 6. No new matter has been added by the amendment to Claim 1.

Also submitted herewith are new Claims 20-24. In new Claim 20, the data-path circuit is limited to output read data in synchronization with a second clock. The second clock corresponds to "RE_CLK" shown in FIG. 6. New Claims 21 and 22 are based on original Claim 17 with clarifying modification. New claims 23 and 24 are based on original Claim 18 with clarifying modification. No new matter has been added by the submission of new Claims 20-24.

Briefly recapitulating by reference to non-limiting corresponding parts disclosed in Applicants' specification, the ECC control apparatus recited in Claim 1 comprises an ECC controller 1 which interrupts a bus between host 3 and NAND memory 2. ECC controller 1, which does not receive a clock from host 3, but uses a first clock generated from a write-enable signal, inserts an error-correction code to write data. Thereafter, ECC controller 1 outputs the write data to NAND memory 2 in synchronization with a first clock.

The claimed structure realizes addition of ECC controller 1 which performs an ECC process relative to NAND memory 2 after the system of host 3 is implemented, without changing the circuit of host 3 that writes data into NAND memory 2.

Kanazawa does not arrange ECC circuit 4 so as to interrupt a data bus. Thus, Kanazawa cannot achieve addition of ECC circuit 4 without changing the circuits of host 1 and memory 3.

Further, in Kanazawa, a system clock is input into ECC controller 50 (FIG. 14), and ECC controller 50 generates an internal clock from the system clock. Kanazawa supplies write data to memory 3 in synchronization with the internal clock. Thus, if a system clock is not supplied, write data cannot be supplied to memory 3. In contrast, the claimed invention does not require a system clock since a clock is generated from an enable signal, as stated in the last paragraph of amended Claim 1. Accordingly, it is respectfully submitted that amended Claim 1 patentably defines over Kanazawa. Furthermore, as the deficiencies of Kanazawa are not believed to be remedied by Kayatama, it is respectfully submitted that the amended claims patentable define over the cited prior art.

Consequently, in view of the present amendment and in light of the above comments, no further issues are believed to be outstanding, and the present application is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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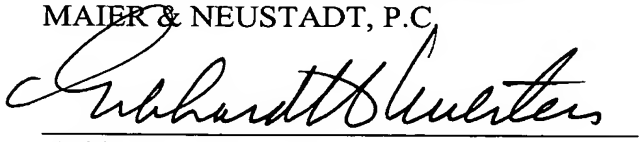

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